11450.2 Reference Section	RCDR Topic	RCDR Number
Paragraph 2-5.6 (a), (c), (d) and 2-5.15(e)	Requirements for microprocessor drives as they apply to PLCs	25-008

QUESTION

Q: NAVCRANECENINST 11450.2A paragraph 2-5.6 (a), (c), (d) and 2-5.15(e), and predecessors, Crane Safety Advisory (CSA) 121 and 121A were promulgated to provide protection, enhance practical redundancy, and reduce the risk of a catastrophic failure due to a microprocessor component failure. The requirements were developed after numerous microprocessor related failures described in the aforementioned CSAs. Microprocessors are utilized in both drives and programmable logic controllers (PLCs). However, these requirements do not address PLCs; clarification of applicability to PLCs is required. Can the applicability of the reference paragraphs/subparagraphs to PLCs be clarified?

ANSWER

A:

1. The requirement in NAVCRANECENINST 11450.2A, paragraph 2-5.6(a) requiring a separate control system (microprocessor drive) for each motion does not pertain to PLCs. One PLC may provide control logic inputs/outputs (I/O) for multiple microprocessor drives or there may be multiple PLCs providing control logic I/O for multiple microprocessor drives.

2. As required by NAVCRANECENINST 11450.2A, paragraph 2-5.6(c), all emergency stop pushbuttons shall remove power from all motors, brakes, and microprocessor drives. This includes any PLCs providing control functionality.

3. As required by NAVCRANECENINST 11450.2A, paragraph 2-5.6(d), emergency stop pushbutton circuitry shall be independent of microprocessor drives. This includes any PLCs providing control functionality.

4. NAVCRANECENINST 11450.2A paragraph 2-5.15(e) requires hoist secondary upper limit switches to be independent of the microprocessor drive. This secondary upper limit switch may be controlled by the PLC if the primary upper hoist limit switch is controlled by the microprocessor drive, and those two limit switches are wired such that it would take two independent failures (e.g., both the microprocessor drive and the PLC must fail) for the anti-two-block (secondary upper limit) function to be rendered inoperative. Otherwise the secondary limit switch must be wired independent of the microprocessor drive and the PLC.

5. Additional NAVCRANECENINST 11450.2A requirements not identified above that apply to microprocessor drives (e.g., parameters, support) also apply to PLCs.